IN THE CLAIMS

Please amend the claims as follows:

1. (original) A receiver comprising means (14) for demodulating a received signal to produce an uncorrected demodulated signal, a dc offset voltage correcting circuit (22) having an output (28) for a corrected signal and a data recovery circuit (42) coupled to the output, the dc offset voltage correcting circuit (22) comprising an input for the uncorrected demodulated signal ($v_{in}$), a bit slicer (30) for detecting received data, filtering means (32) for regenerating the demodulated signal less noise and dc offset, subtracting means (34) for subtracting the regenerated demodulated signal from the uncorrected demodulated signal to produce the dc offset voltage ($v_{off}$) and a feedback circuit for feeding back the dc offset voltage to the bit slicer.

2. (original) A receiver as claimed in claim 1, characterised in that the filtering means (32) is a low pass filter having a characteristic substantially the same as the transfer function of at least the complete receiver chain.

3. (original) A receiver as claimed in claim 2, characterised by delay means (38) for delaying the uncorrected demodulated signal by

at least the duration of the time delay due to the transmission of a signal through the filtering means.

4. (currently amended) A receiver as claimed in ~~any one of claims 1 to 3~~claim 1, characterised in that the feedback circuit includes a low pass filter (40).

5. (currently amended) A receiver as claimed in ~~any one of claims 1 to 3~~claim 1, characterised in that the feedback circuit includes a variable bandwidth filter controlled by the estimated rate of drift.

6. (currently amended) A receiver as claimed in ~~any one of claims 1 to 5~~claim 1, characterised by another subtracting stage (24) having a first input (25) for the uncorrected demodulated signal ($v_{in}$) and a second input (26) for the dc offset voltage ($v_{off}$) and an output (27) coupled to the bit slicer (30) and to the data recovery circuit (42).

7. (original) A method of dc offset voltage correction in a demodulated signal, comprising obtaining a dc free estimate of the demodulated signal, subtracting the dc free estimate of the demodulated signal from a substantially contemporaneous version of

the demodulated signal to obtain a dc offset voltage and subtracting the dc offset voltage from the demodulated signal.

8. (original) A method as claimed in claim 7, characterised by bit slicing a difference signal formed by subtracting the dc offset voltage from the demodulated signal to provide an estimate of the demodulated signal and by filtering the estimate of the demodulated signal to obtain a dc free estimate of the demodulated signal.

9. (currently amended) A method as claimed in claim 7~~ or 8~~, characterised by filtering the dc offset voltage.

10. (currently amended) A method as claimed in claim 7~~ or 8~~, characterised by delaying the demodulating signal prior to subtracting the dc free estimate of the demodulated signal.